IN THE CLAIMS:

The following is a listing of the claims of the present application:

1. (Currently Amended) A method of performing add-compare-select operations in accordance with a Viterbi decoder, the method comprising the steps of:

respectively adding input values of two or more sets of input values to generate sums for the two or more sets;

substantially concurrent with the respective addition of the input values of the two or more sets of input values, comparing the two or more sets of input values, wherein the comparison operation comprises performing carry save addition on the two sets of input values, and evaluating a carry output of the carry save addition operation to make the determination as to which set of the two or more sets would yield a particular result; and

selecting one of the generated sums of the two or more input sets based on the comparison operation performed on ~~of~~ the two or more sets of input values.

2. (Original) The method of claim 1, wherein the comparison operation further comprises comparing the two or more sets of input values to make a determination as to which set of the two or more sets would result in the largest sum.

3. (Canceled).

4. (Currently Amended) The method of claim ~~3~~ 1, wherein the carry save addition operation is performed by one or more data compressors.

5. (Original) The method of claim 1, wherein one input value of each set of input values is a previously computed path metric and the other input value of each set of input values is an appropriate branch metric such that the generated sum of the input values represents a new path metric which may potentially be selected based on the substantially concurrent comparison operation.

6. (Original) The method of claim 1, wherein the comparison operation begins when the input values of the two or more sets are available such that the comparison operation is completed before completion of the addition operation.

7. (Currently Amended) Apparatus for performing add-compare-select operations in accordance with a Viterbi decoder, the apparatus comprising:

at least one processor operative to: (i) respectively add input values of two or more sets of input values to generate sums for the two or more sets; (ii) substantially concurrent with the respective addition of the input values of the two or more sets of input values, compare the two or more sets of input values, wherein the comparison operation comprises performing carry save addition on the two sets of input values, and evaluating a carry output of the carry save addition operation to make the determination as to which set of the two or more sets would yield a particular result; and (iii) select one of the generated sums of the two or more input sets based on the comparison operation performed on ~~of~~ the two or more sets of input values; and

a memory, coupled to the at least one processor, for storing at least a portion of results associated with one or more of the add, compare, select operations.

8. (Original) The apparatus of claim 7, wherein the comparison operation further comprises comparing the two or more sets of input values to make a determination as to which set of the two or more sets would result in the largest sum.

9. (Canceled).

10. (Original) The apparatus of claim 7, wherein one input value of each set of input values is a previously computed path metric and the other input value of each set of input values is an appropriate branch metric such that the generated sum of the input values represents a new path metric which may potentially be selected based on the substantially concurrent comparison operation.

11. (Original) The apparatus of claim 7, wherein the comparison operation begins when the input values of the two or more sets are available such that the comparison operation is completed before completion of the addition operation.

12. (Currently Amended) A Viterbi decoder for performing an add-compare-select algorithm, the algorithm comprising the steps of:

respectively adding input values of two or more sets of input values to generate sums for the two or more sets;

substantially concurrent with the respective addition of the input values of the two or more sets of input values, comparing the two or more sets of input values, wherein the comparison operation comprises performing carry save addition on the two sets of input values, and evaluating a carry output of the carry save addition operation to make the determination as to which set of the two or more sets would yield a particular result; and

selecting one of the generated sums of the two or more input sets based on the comparison operation performed on ~~of~~ the two or more sets of input values.

13. (Original) The Viterbi decoder of claim 12, wherein the comparison operation further comprises comparing the two or more sets of input values to make a determination as to which set of the two or more sets would result in the largest sum.

14. (Canceled).

15. (Currently Amended) The Viterbi decoder of claim 12, wherein the ~~add-compare-select algorithm is implemented in accordance with~~ Viterbi decoder comprises an integrated circuit device.

16. (Currently Amended) An article of manufacture for performing add-compare-select operations in accordance with a Viterbi decoder, the article comprising a machine readable medium containing one or more programs which when executed implement the steps of:

respectively adding input values of two or more sets of input values to generate sums for the two or more sets;

substantially concurrent with the respective addition of the input values of the two or more sets of input values, comparing the two or more sets of input values, wherein the comparison operation comprises performing carry save addition on the two sets of input values, and evaluating a carry output of the carry save addition operation to make the determination as to which set of the two or more sets would yield a particular result; and

selecting one of the generated sums of the two or more input sets based on the comparison operation performed on ~~of~~ the two or more sets of input values.

17. (Original) The article of claim 16, wherein the comparison operation further comprises comparing the two or more sets of input values to make a determination as to which set of the two or more sets would result in the largest sum.

18. (Canceled).

19. (Currently Amended) An integrated circuit device, the integrated circuit device comprising a Viterbi decoder operable to:

respectively add input values of two or more sets of input values to generate sums for the two or more sets;

substantially concurrent with the respective addition of the input values of the two or more sets of input values, compare the two or more sets of input values, wherein the comparison operation comprises performing carry save addition on the two sets of input values, and evaluating a carry output of the carry save addition operation to make the determination as to which set of the two or more sets would yield a particular result; and

select one of the generated sums of the two or more input sets based on the comparison operation performed on ~~of~~ the two or more sets of input values.

20. (Original) The integrated circuit device of claim 19, wherein the comparison operation further comprises comparing the two or more sets of input values to make a determination as to which set of the two or more sets would result in the largest sum.

21. (Canceled).